REMARKS AND ARGUMENTS

Allowed claims

The Examiner has allowed claims 2-20 and 22-26. These claims are patentable over the cited art of record.

Rejection under 35 USC §102

Claim 1 is rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,546,461 (Au et al.). Applicant respectfully disagrees.

Claim 1, by way of this response, has been amended to more clearly recite the invention. As amended, claim 1 recites an IC comprising a memory cell array having a plurality of memory cells, wherein each memory cell includes at least first and second ports forming a memory cell array with at least first and second access ports for accessing the memory cells. A cache memory is coupled to the first and second access ports, wherein during a read operation to the memory cell array to obtain read data through one of the first and second access ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory. The IC further comprises a refresh control circuit for performing refresh operations. The refresh control circuit, during a memory access conflict between the read and refresh operations, allows both read and refresh operations to be performed if the read data is stored in the cache memory.

Au et al. (Au), on the other hand teaches a multi-port cache memory device coupled to an embedded SRAM array. *See* Au, Fig. 1. Au, however, nowhere teaches or suggests the use of a refresh control circuit. Furthermore, Au nowhere teaches or suggests the use of a refresh control circuit, which during a memory access conflict between the read and refresh operations, allows both read and refresh operations to be performed if the read data is stored in the cache memory. This fact is acknowledged by the Examiner in page 4 of the Office Action mailed on April 13, 2007. In particular, the Examiner stated that "Au et al. (U.S. Patent No. 6,546,461), and others, do not teach the claimed

invention…wherein during a conflict between a read operation to the memory array and a refresh operation, the cache memory provides read data if the read data is contained there or the read operation is stalled until the conflict is over if the read data is not contained in the cache memory." Therefore, Applicant submits that claim 1, as amended, is patentable over Au and respectfully requests withdrawal of the rejection based on 35 USC § 102.

Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

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Respectfully submitted,

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